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(54) Title: METHOD OF PATTERNING RESIST FOR PRINTED WIRING BOARD

(57) Abstract

A methof for patterning a photoresist or insulating layer on a printed wiring board utilizes two photoreactive coatings comprising a photoprocessable ultraviolet (UV) sensitive layer overlaid with a thin, unexposed, undeveloped strip base silver film. A white light x-y plotter, preferably employing an octogonal aperture, is driven directly from a CAD system to expose the film on the board in the desired pattern without affecting the underlying UV sensitive layer. The film is then developed on the board and employed as an *in situ* mask for the underlying UV layer during exposure of the board to a UV flood lamp. After UV exposure the film is peeled off to allow conventional processing of the selectively polymerized layer. This technique produces high resolution, inspectable onboard masks in full registration using reliable low energy plotters.

METHOD OF PATTERNING RESIST FOR PRINTED WIRING BOARD

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to copending application Serial No. 742,747 filed June 10, 1985 (the same day as the present application) by Grandmont and Lake entitled "Multilayer Circuit Board Fabrication Process", assigned to the assignee of the present application and incorporated herein by reference.

BACKGROUND OF THE INVENTION

The invention relates generally to the manufacture of printed wiring boards for electrical components and more particularly to photoprocessing techniques for printed wiring boards.

The ongoing integration and miniaturization of components for electronic circuitry has become a growing challenge to the limits of printed wiring board technology over the last twenty years. Printed circuit boards or printed wiring boards (PWB) as they are more accurately termed, play several key roles. First, the electrical components, such as specially packaged integrated circuits, resistors, etc., are mounted or carried on the surface of the flat usually sturdy card-like board. Thus, the PWB serves as a support for the components. Secondly, using chemically etched or plated conductor patterns on the surface of the board, the PWB forms the desired electrical interconnections between the components. In addition, the PWB can include a metal area serving as a heat sink.

Conductor patterns are typically formed by photoetching a copper foil clad epoxy fiberglass substrate. A photoresist layer is applied to the copper foil and patterned by exposure to untraviolet (UV) light projected through a mask, often referred

to as "artwork". Areas exposed on the photoresist are polymerized. The unpolymerized areas are removed by a chemical solution leaving areas of copper, the desired conductor pattern, underneath the protective barrier of the remaining polymerized hardened photoresist. The exposed copper is then etched away and the remaining photoresist is chemically removed to expose the resulting conductor pattern. Alternatively, the photoresist can be patterned to form channels for electroless plating of conductor patterns. There are, of course, many variations on this procedure, but all of them require photo-patterning of the resist layer.

As the use of integrated circuits has grown, the higher density of interconnection terminals for inputs and outputs (I/O) has necessitated double-sided PWB's in which additional interconnections are made employing conductor patterns on the other side of the board.

Along with increased circuit integration, surface mount technology (SMT) has accelerated the densification of electronic circuitry. Surface mount devices (SMD) are applied directly to the surface of the PWB and soldered using vapor phase, infra-red (IR) or other techniques. SMT is revolutionizing the electronics manufacturing industry by reducing assembly cost by about 50%, increasing component density by over 40% and enhancing reliability. The array of terminals on SMD's has a higher density or finer pitch than those on conventional components. As each terminal still has to be properly electrically connected to the respective conductor on the board, registration of SMD's requires high resolution for the PWB conductor lines. Indeed, SMD circuitry has become so dense that double-sided boards cannot accommodate all of the needed electrical connections. Thus, multilayer PWB's have become the focus of attention and several

competing technologies are evolving. Those technologies which rely on stacks or layers of conductor patterns have interlayer registration requirements in addition to the exacting line width and spacing of a conductor pattern in a given layer. Manufacturing very fine lines on the order of 3 to 5 mils in registration over four or more layers deep is very difficult.

To take fullest possible advantage of the benefits offered by the emerging SMT, new fabrication processes must be developed in the manufacture of substrates and boards. In the past, one of the problem areas in fabrication of PWB's has been the generation and use of artwork masters for patterning the photoresist layers. Using photographic film or glass plates poses inherent difficulties in stability, registration, transport and storage.

The elimination of artwork masters from the board fabrication process has long been an industry goal, one which fostered the development of high-speed UV laser plotters. Several machines are currently available; all are very expensive and in an early stage of development. These machines pattern the UV sensitive resist directly without artwork. Conductor patterns are designed using computer-assisted design (CAD) which digitizes the coordinates and dimensions of all of the paths and converts them to control signals for a UV laser x-y plotter. In addition to their very high cost, these systems have a number of limitations which become significant in fine line, high density work. Principal among these is the fact that UV sensitive resists are low contrast materials, requiring high levels of exposure energy. As a result, line edge resolution is limited. In order to achieve high plot speeds, these systems all operate in a raster scan mode. Raster scanning produces considerable edge irregularities which are very apparent in plotting angled

lines. Limitations in accuracy and minimum line width are characteristic of these raster plotting systems. Another problem area in current systems is the short life expectancy of the laser source. A further problem with direct from CAD UV plotting of the photoprocessable layer is that it does not permit inspection before polymerization. If an error is made in the plot, the mistake is automatically embedded in the UV sensitive layer. In the case of a resist, the board may be salvaged only by removing the entire resist layer and starting over after cleaning and baking the board free of moisture a second time. In the case of a UV plotted solder mask, a glitch in the pattern results in the entire panel being discarded.

SUMMARY OF THE INVENTION

Accordingly, the general object of the invention is to eliminate separate artwork masters which must be manipulated in the board fabrication process while avoiding the edge resolution problems of direct UV plotters. A further object of the invention is to provide extremely fine line patterning with minimal interlayer misregistration at lower cost and higher speed, using inherently more reliable equipment.

These and other objects of the invention are achieved by a system which offers a highly simplified means of substrate/board fabrication driven directly from a CAD layout. The process utilizes a very thin high contrast photosensitive strippable film laminated directly onto a substrate coated with a photoprocessable layer such as resist or a permanent insulating material. Alternatively, the photoprocessable layer and film are co-laminated initially and applied as a composite to the substrate. The resulting structure can be exposed onboard from CAD using a conventional low energy white light plotter which cannot effect significant polymerization in the underlying resist

layer. After exposure, the film layer is developed onboard using conventional film developing chemistry or another process appropriate to the film type used. Development does not disturb the underlying resist. The resultant high contrast film image forms an in situ mask for subsequent uniform UV flood exposure of the underlying resist. After UV exposure, the film is removed, preferably by peeling it off of the substrate. Further processing of the substrate may be carried out by conventional means. The process can be repeated for multiple layering with no registration errors induced by manipulating separate artwork masters. The system may also employ a raster scan plotter. An octagonal spot makes straight edged lines at 45° or 90° to the scan direction. Because the film exhibits high contrast, low intensity light is adequate for exposure, yielding extremely fine resolution unlike direct UV patterning of the underlying resist. Thus, the invention combines the benefits of CAD driven plotters with onboard direct pattern formation but yields a sharper pattern by virtue of using high contrast, low energy, white light plotting. Moreover, the visible image on the developed film is fully inspectable before UV exposure and available for touch up if necessary. If the image is unacceptable, the film can be peeled off and unexposed film reapplied. The system also can be used to pattern solder masks or permanent dry film insulating layers, and the like, in the same manner as for resists.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A-1G are diagrammatic cross-sectional views of a PWB undergoing a sequence of steps for patterning the photoresist directly from CAD using an etched pattern subtractive technique.

FIG. 2 is a diagrammatic functional representation of a system for prelaminating the resist and photographic film together before application to a substrate as a composite.

FIG. 3 is a diagrammatic functional representation of a system for applying the photographic film to a resist coated substrate.

FIGS. 4A-4F are diagrammatic cross-sectional views of a printed wiring board undergoing application of permanent dry film patterned in a sequence of steps according to the invention.

FIGS. 5A-5F are diagrammatic cross-sectional views of a patterning sequence according to the invention utilizing the standard pattern plating process.

FIGS. 6A-6B are diagrammatic representations of an equilateral octagonal spot raster scan photoplotter according to the invention.

FIGS. 7A-7B are diagrammatic representations of a nonequilateral octagonal spot raster scan photoplotter according to the invention.

DETAILED DESCRIPTION

As shown in Fig. 1A, the design of a conductor pattern for a layer of a PWB is rendered on CAD 10. The PWB may be any size up to a typical maximum of 18 by 24 inches. The coordinates of the pattern are digitized and transmitted in a compatible digital form as the control input to an x-y plotter 12, for example, a Gerber Model 35. Plotters of this type, typically used for making artwork masters, have a moving table (not shown) to which the film is affixed. The table is capable of translational motion simultaneously in the x and y axes by means of separate x and y stepper motors and screw drives. The plotting head consists of a white light source 14 with a number of selectable apertures and in the present case a yellow filter

16 to remove the unwanted UV component. The plotter is set up in a dark room and the beam of light 18, moving relative to the film, "writes" a pattern of lines, usually of varying widths, on the film.

As shown in Fig. 1A, substrate 20, for example, an epoxy fiberglass sheet, carries a uniform layer of metal, e.g., copper 22. A photoresist layer 24 sensitive to UV light is superimposed on the copper layer 22. A thin sheet of strip base photographic film 26 overlays the photoresist 24. Film 26 is preferably one-quarter to one-half mil thick.

The composite structure 30 of Fig. 1A can be prepared in several different ways. As shown in Fig. 2, the resist 24 and film 26 can be laminated by hot rolling at 32 to form a composite two ply sheet 34 which is then roll-laminated at 36 onto an uncoated substrate 38. Alternatively, as shown in Fig. 3, the photographic film 26 can be roll-laminated directly to a resist coated substrate.

In either case, the resulting structure 30 is mounted on the moving table (not shown) of the plotter 12 and the film 26 is exposed by the beam 18.

Once exposed, the film 26 is developed (Fig. 1B) using conventional photographic developing chemistry, for example, by immersing the entire structure 30 in the required sequence of baths in the darkroom. The image 42 develops in the upper emulsion layer of the thin film 26.

The film 26 may be a strip base silver film. A suitable film in negative or positive working form is available from The 3-M Company. Chemical development of the film does not

affect the integrity of the particular underlying resists used, preferably semi-aqueous or solvent-type resist.

A possibly superior film for use in connection with this invention is a dry silver imaging film. This type of film, also available from The 3-M Company, is photosensitive to white light and has relatively high contrast, but does not require chemicals for development of the image. The image is developed by heating the film either at elevated temperatures for a brief period or at relatively moderate temperatures for a longer period of time. Because of this property, dry silver film has very poor archival properties as it becomes fogged after a period of time even at moderately elevated temperatures. This type of film may be ideal, however, for the present invention because it can be applied with the emulsion side down in contact with the substrate, e.g., the resist or solder mask. By placing the emulsion side directly against the photoprocessable layer, the in situ mask properties are enhanced because after the mask, the UV does not have to pass through the film substrate material which carries the emulsion. In other words, the UV is masked by the film image in the emulsion immediately before entering the UV sensitive layer. A possible disadvantage of the dry silver film in this process is that it exhibits lower contrast than strip base film developed by conventional chemistry. In addition, while the developed dry silver film is inspectable on board before UV exposure, it cannot be easily retouched.

After the image 42 is fixed in the film 26, the composite structure 30 is exposed to a UV flood lamp 44, as shown in Fig. 1C. The darkened areas 42 in the image of the film 26 absorb the ultraviolet light and shield the underlying resist. Where the film 26 remains transparent, however, the ultraviolet light passes to the resist layer 24 and polymerizes the

underlying portions 46. In practice, it is believed to be desirable to use a short burst of UV energy from a flash lamp to yield more uniform polymerization.

After the board is removed from the UV exposure apparatus 44, the next step, as shown in Fig. 1D, is to peel off the film 26. Once the film 26 is removed, the patterned photoresist 24 is uncovered. The remainder of the processing of the substrate is by conventional means (resist development, etching or plating, etc.). As shown, for example, in Figs. 1E, 1F and 1G, the unpolymerized portions of the photoresist 24 may be removed by chemical action leaving only the polymerized portions 46 over selected areas of the copper layer 22. Next, the copper is etched to form copper conductor patterns 48 and, as shown in Fig. 1G, the polymerized portions of the resist 46 are chemically removed leaving the copper conductor patterns 48 specified by the original CAD design.

The present invention is also applicable to the preparation of solder masks and insulating layers. As shown in Figs. 4A-4E, a copper foil clad substrate 20' of epoxy fiberglass or other suitable material is patterned using a conventional technique or the technique of the invention shown in Figs. 1A-1G. The conductor foil pattern 50 is shown in Fig. 4A. A composite 52 of strip base silver film 26 and permanent dry film (PDF) 54, roll-laminated together in the manner of Fig. 2, is applied directly to the substrate 20' covering the conductive pattern 50. Alternatively, the PDF 54 can be applied first to form a coated substrate to which the film 26 is then applied in the manner of Fig. 3.

As shown in Fig. 4C, the composite covered structure is subjected to the same steps as shown in Figs. 1A, 1B, 1C and 1D.

The direct from CAD plotted image 55 formed in the emulsion layer of the film 26 selectively shields the underlying regions of the PDF over the conductive foil pattern 50, serving as an in situ mask. In Fig. 4D, the unexposed unpolymerized areas of the PDF over the conductive pattern 50 are removed chemically leaving the polymerized hardened PDF insulating layer 60.

The exposed metal sites in Fig. 4D may be coated with solder by immersion in a molten solder bath to fill up the voided channels or apertures in the insulating layer 60 with solder 62 (Fig. 4E). To achieve a flush surface, the top layer of the structure is exposed to a hot air knife which reflows the top surface of the solder 62. The result is a smooth surface ready for the attachment of SMD's. In practice, solder paste is screened onto the surface of the structure in Fig. 4E, the SMD's are mounted and the structure is heated in a vapor phase process, for example, to form electrical connections between the board conductors and the SMD's.

As shown in Fig. 4F, alternatively, the PDF can be employed as an interlayer insulator in multilayer structures of the type disclosed in our above-referenced copending multilayer application. The copper foil pattern 50 of Fig. 4D forms catalytic sites for electroless plating. The channels formed in the PDF insulating layer 60 are plated up electrolessly to make solid copper conductors 64 (Fig. 4F). Subsequent layers would be applied on top of the structure shown in Fig. 4F to build up a multilayer circuit.

A pattern plating method is shown in Fig. 5A-5F employing the direct from CAD in situ photo-mask technique of the present invention. As shown in Fig. 5A, a substrate 20 carries an upper layer of foil 22, a resist layer 24 and an image

developing film layer 26. The configuration is identical to that shown in Fig. 1A, except that, when using a negative working resist, the film is preferably a negative-type strip base film rather than a positive-type strip base film as shown in Fig. 1A.

The film layer is exposed (plotted) and developed on the board as shown in Fig. 5B to produce the image 70. The board is then exposed to a UV source to polymerize the unshielded portions of the resist layer 24. As indicated in Fig. 5B, the film 26, having served its purpose, is peeled off and discarded. Next, the unpolymerized resist is removed in Fig. 5C leaving areas of hardened resist 72 above the uniform layer of copper 22.

Because the copper layer is intact, electroplating can be employed. Through holes (not shown) are plated along with the copper channels exposed through the resist. Those areas covered by resist 72 are not affected by electroplating. This is advantageous since, as only the conductor pattern (and holes) are plated, there is no extraneous electroplated copper to be removed.

As shown in Fig. 5D, after the copper conductors 22' are electroplated, a coating 74 of tin-solder is electroplated in an appropriate bath onto the upper surface of the copper conductors 22'. The tin-solder coating 74 clads the desired conductor pattern. After removing the hardened polymerized resist 72 as shown in Fig. 5E, the structure is placed in an etching bath. The tin-solder coating 74 acts as a resist to the copper etchant. As a result, the copper foil layer 22 is removed everywhere except where the pattern has been plated with tin-solder, thus leaving the desired tin-clad copper pattern as shown in Fig. 5F. Following the final step illustrated in the drawing (Fig. 5F), the structure is heated by IR or hot oil

treatment to reflow the tin-solder layer 74 over the etched edges 76 (Fig. 5F) of the copper pattern.

The advantages of direct from CAD photo-plotting onto an in situ silver film mask are numerous. In particular, a very thin high contrast in situ film mask yields high resolution patterning capability far exceeding direct from CAD UV plotting of the resist. Direct from CAD exposures can be performed using standard low cost white light photoplotters as opposed to high cost complex UV plotting systems requiring high energy UV lasers which need frequent replacement. Moreover, high contrast white light plotting is superior to UV plotting because light sensitive film exhibits higher contrast at lower energy levels.

The photoplotted in situ mask provides the basis for high precision interlayer registration and multilayer printed wiring boards. The film exposure is inspectable and stable prior to resist exposure.

Inspectability is a particularly important advantage over UV plotting. An error or artifact in the UV polymerized pattern cannot easily be surgically removed. Instead, the resist must be dissolved away and reapplied after cleaning and drying the board, or the board must simply be discarded. In manufacturing electrolessly plated multilayer boards with the process disclosed in the above-referenced copending application, the consequences of misplotting UV sensitive PDF layers are serious indeed. Using the present process, however, the onboard developed film can be easily checked for artifacts produced by a plotting glitch, hair, dust, etc. In many cases instead of peeling the old film off and reapplying new film, the in situ photo-mask can be retouched by using a UV opaque fountain pen or by excising tiny portions of falsely exposed emulsion with an

exacto knife. In any event, if necessary, the bad mask can be quickly peeled off to try again with a new piece of film. The important difference is that the UV sensitive layer remains undisturbed even though the board is directly plotted from a CAD layout.

The system can be further adapted to a high speed raster scan system for production use without any of the limitations of current laser equipment. A white light source under consideration is a Xenon strobe lamp, beam collimated.

The use of an octagonal aperture for the raster scan beam eliminates any edge irregularity on both 45 and 90° lines, as well as 0° lines, i.e., parallel to the scan direction. As shown in Fig. 6A and 6B, a raster scan plotter can be equipped with a simple white light source with an octagonal aperture preferably in the form of a stencil. The octagonal spot is focused on the emulsion in the film. In Fig. 6A, the scan direction is along the y axis as indicated and the objective is to draw or image a line in the x direction. To accomplish this, the strobe lamp is triggered at precisely the correct y coordinate (y_1 in Fig. 6A) to expose an octagon 90 on the film during a first scan. In the next scan, the strobe lamp is flashed, again at position y_1, to expose a second octagon image 92 as shown. The interscan spacing, is approximately one-third of the width of the octagon as shown so that the sides 90a and 92a, for example, are aligned and touching or just overlapping. After consecutive scans, the resulting staggered, overlapping octagons plot a line with well delineated, straight edges. In addition, as shown in Fig. 6B, diagonal lines on 45° angles also result in patterns with straight edges 94a, 96a formed by octagon spots on successive scans in the y direction spaced at one-third spot widths.

As the octagons shown in Figs. 6A and 6B are equilateral or regular octagons, the amount of overlap at the sides is greater for the 90° path (Fig. 6A) than for the 45° path (Fig. 6B). This effect can be eliminated by employing diagonal sides, relative to the scan direction, in equal lengths which bear a ratio of approximately the square root of two to the orthogonal sides as shown in Figs. 7A and 7B. In this design, the octagon will be evenly divided into thirds so that the overlap will be identical when making diagonal and orthogonal lines. However, if the width of the orthogonal line is 3 units, the width of the resulting diagonal line would be 2.828 units. The widths could be made equal, however, by changing the magnification if the raster plotter had an automatic zoom lens, for example, or by proper adjustment of the duration of the exposure to allow the light to sweep out a slightly extended octagon in the Y-direction to compensate for its diminished diagonal width when constructing diagonal lines.

Existing raster systems including the foregoing refinements and the in situ silver film mask system will yield a practical high quality substrate manufacturing process with production speeds realistically approaching five seconds per plot.

The in situ mask system can accommodate positive or negative type strip base film. Since the majority of available resists used today are negative working, positive strip base film is preferred for subtractive processes. Negative-type strip base film would be used in an identical manner if the boards were fabricated using a pattern plating process as shown in Figs. 5A-5F with negative working resist.

The foregoing description of the in situ film mask PWB system is intended to be illustrative and not restrictive. For

example, although the foregoing examples show only single sided boards, double sided boards can be made by applying the same process simultaneously or in sequence to both sides of a substrate. Many variations on or additions to the steps or materials described herein are, of course, possible without departing from the principles or spirit of the present invention, the scope of which is indicated by the appended claims and their equivalents.

We claim:

1. A process for patterning a photoprocessable layer on a printed wiring board substrate, comprising

preparing a substrate with an upper layer of photoprocessable material sensitive to a first spectrum of directed energy,

applying a layer of unexposed, undeveloped photographic imaging film sensitive to a second spectrum of directed energy to the substrate over the photoprocessable layer,

selectively exposing said film on the substrate with an automatic photoplotter emitting a beam including said second spectrum and substantially excluding said first spectrum so that the film is activated without affecting the underlying layer of photoprocessable material,

developing the film on the substrate,

exposing the photoprocessable layer to energy in said first spectrum distributed substantially uniformly over the substrate through the image developed in said film layer as an in situ mask,

removing said film layer, and

processing said photoprocessable layer,

whereby low energy plotting can be used to create high resolution inspectable onboard masks.

2. The process of claim 1, wherein said step of removing said film is accomplished by peeling said film off of said substrate.

3. The process of claim 1, wherein processing said photoprocessable layer after exposure is accomplished by chemically removing either the exposed or unexposed portions of said photoprocessable layer.

4. The process of claim 1, wherein said first spectrum is UV and said second spectrum is visible light.

5. The process of claim 1, wherein said step of exposing said film with an automatic photoplotter includes the preliminary step of preparing a digital representation of a conductor pattern and controlling said photoplotter by means of said digital representation.

6. The process of claim 5, wherein said photoplotter is a white light x-y plotter.

7. The process of claim 5, wherein said photoplotter is a raster scan plotter with a triggerable white light source.

8. The process of claim 7, wherein said white light source is applied to the film in the shape of an octagon and the interscan distance is such that sides of octagons in adjacent scans are aligned and in substantial contact with each other to form a straight edged line at 0, 45 or 90° to the scan direction.

9. The process of claim 1, wherein said film is applied with its emulsion-side adjacent said photoprocessable layer.

10. The process of claim 1, wherein said film is a dry silver film.

11. The process of claim 1, wherein said film is a heat-developable film.

12. The process of claim 1, wherein said film is a heat-developable film applied with its emulsion side adjacent said photoprocessable layer.

13. A process for patterning a photoprocessable layer for a printed wiring board, comprising

laminating together a layer of photoprocessable material sensitive to directed energy in a first spectrum with a layer of unexposed, undeveloped photographic imaging film sensitive to directed energy in a second spectrum to form a composite,

applying said composite with the film layer on top to a substrate,

selectively exposing said film layer with an automatic photoplotter emitting a beam including said second spectrum and substantially excluding said first spectrum so that the film is activated without affecting the underlying layer of photoprocessable material,

developing the film on the substrate,

exposing the photoprocessable layer to energy in said first spectrum distributed substantially uniformly over the substrate through the image developed in said film layer as an in situ mask,

removing said film layer, and

processing said photoprocessable layer,

whereby low energy plotting can be used to create high resolution inspectable onboard masks.

14. The process of claim 13, wherein said step of removing said film layer is accomplished by peeling said film off of said substrate.

15. The process of claim 13, wherein processing said photoprocessable layer after exposure is accomplished by chemically removing either the exposed or unexposed portions of said photoprocessable layer.

16. The process of claim 13, wherein said first spectrum is UV and said second spectrum is visible light.

17. The process of claim 13, wherein said step of exposing said film with an automatic photoplotter is accomplished by creating a digital representation of a conductor pattern and controlling said photoplotter by means of said digital representation.

18. The process of claim 17, wherein said photoplotter is a white light x-y photoplotter.

19. The process of claim 17, wherein said photplotter is a raster scan photoplotter with a triggerable white light source.

20. The process of claim 19, wherein said light source is applied to the film in the shape of an octagon and the interscan spacing is such that the sides of the octagon are aligned and in substantial contact with each other to form a straight edged line at 0, 45 and 90° to the scan direction.

21. The process of claim 13, wherein said film is applied with its emulsion side adjacent said photoprocessable layer.

22. The process of claim 13, wherein said film is a dry silver film.

23. The process of claim 13, wherein said film is a heat-developable film.

24. The process of claim 13, wherein said film is a heat-developable film applied with its emulsion side adjacent said photoprocessable layer.

25. A raster scan line plotting method, comprising the steps of

directing a triggerable beam of energy onto a film sensitive to said energy in the shape of a polygon, and

triggering said beam at corresponding successive positions in consecutive scans to form a line, the interscan spacing being such that aligned adjacent sides of the exposed polygons are touching so as to form a continuous straight edge to delineate said line when the line is at predetermined angles with the scan direction.

26. The method of claim 25, wherein said polygon is an octagon.

27. The method of claim 26, wherein said predetermined angles include 90° and 45°.

28. The method of claim 27 wherein the length of the sides of the octagon diagonal to the scan direction bear a ratio to the orthogonal sides of approximately 1.4.

29. The method of claim 26, wherein said energy is in the form of white light and said film is a silver film.

30. A composite structure for making a printed wiring board, comprising

a substrate,

an adherent photoprocessable layer on top of said substrate sensitive to directed energy in a first spectrum, and

a layer of unexposed, undeveloped, strippable, imaging film peelably laminated on top of said photoprocessable layer,

said film being sensitive to directed energy in a second spectrum,

whereby low energy plotting can be used to create high resolution inspectable onboard masks.

31. The structure of claim 30, wherein said substrate includes a substrate bearing a patternable conductive layer.

32. The structure of claim 31, wherein said photoprocessable layer is a layer of photoresist.

33. The structure of claim 30, wherein said first spectrum is UV and said second spectrum is visible light.

34. The structure of claim 30, wherein said substrate includes a substrate bearing a surface pattern of conductors.

35. The structure of claim 34, wherein said photoprocessable layer is a patternable permanent insulating layer.

36. The structure of claim 35, wherein said insulating layer is PDF.

37. The structure of claim 35, wherein said insulating layer is solder mask material.

38. The structure of claim 30, wherein said film is applied with its emulsion side adjacent said photoprocessable layer.

39. The structure of claim 30, wherein said film is a dry silver film.

40. The structure of claim 30, wherein said film is a heat-developable film.

41. The structure of claim 30, wherein said film is a heat-developable film with its emulsion-side adjacent said photoprocessable layer.

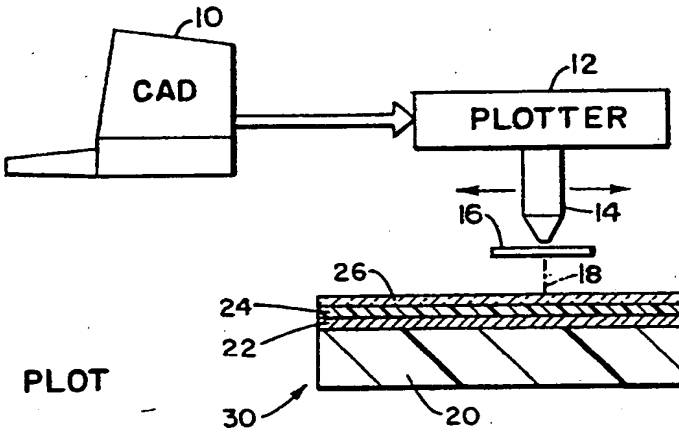


FIG. 1A PLOT

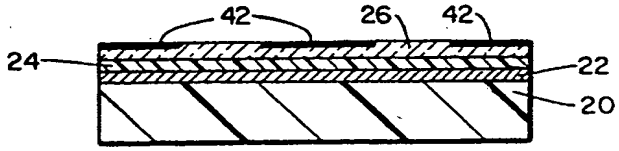


FIG. 1B DEVELOP

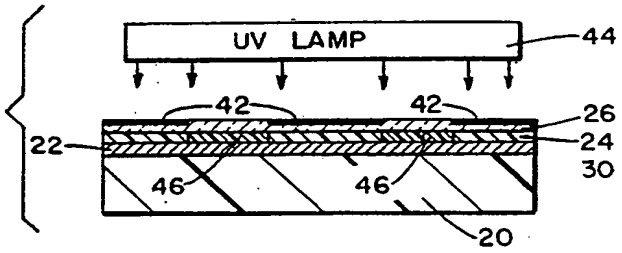


FIG. 1C UV

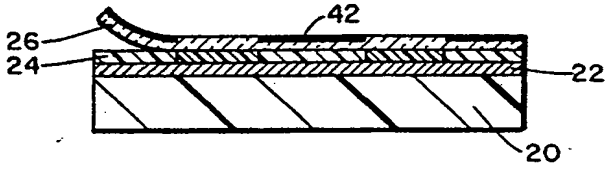


FIG. 1D PEEL FILM

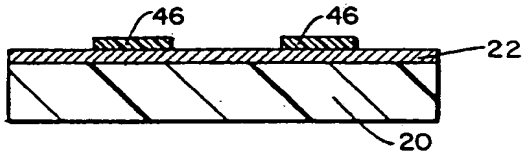


FIG. 1E REMOVE SOFT RESIST

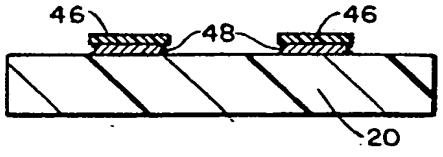


FIG. 1F ETCH Cu

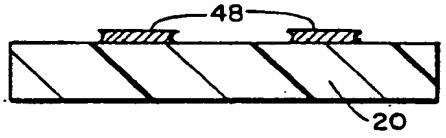
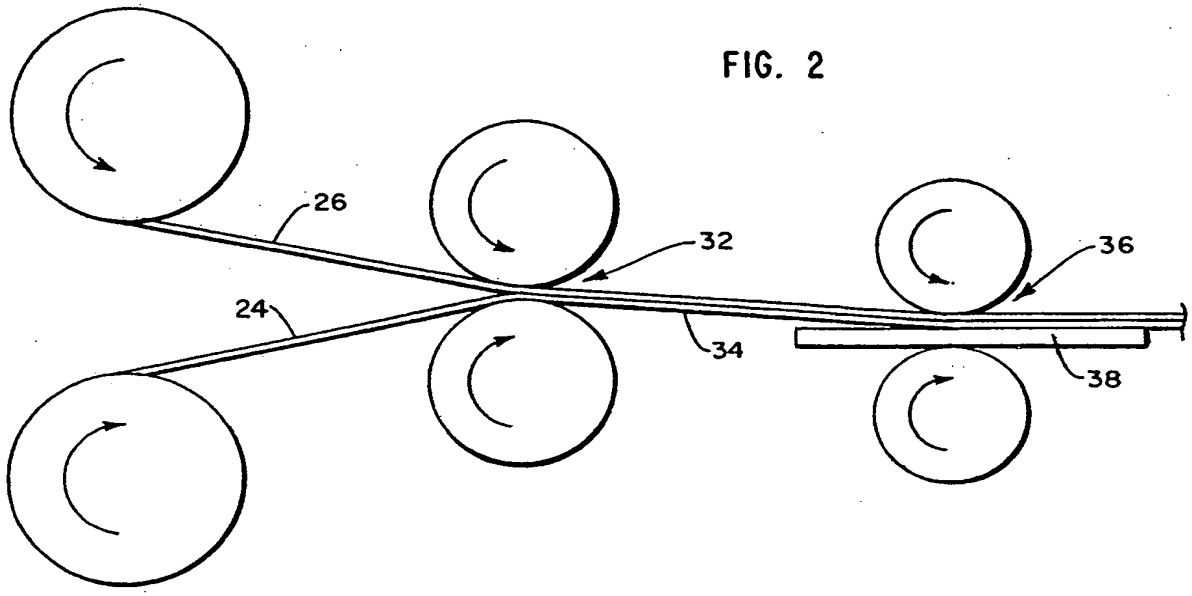


FIG. 1G REMOVE HARD RESIST

FIG. 2



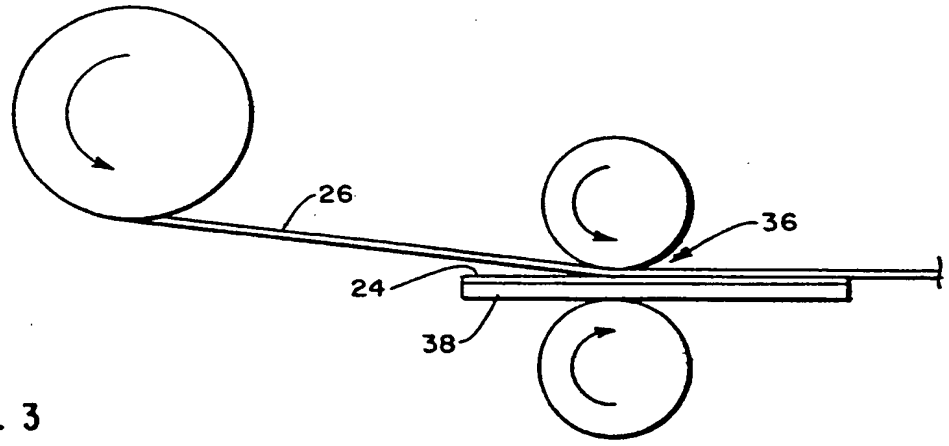


FIG. 3

FIG. 4A PATTERN Cu. FOIL

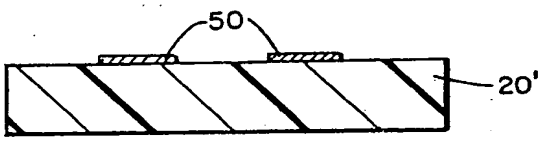


FIG. 4B APPLY FILM/PDF COMPOSITE

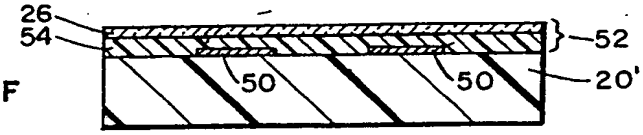


FIG. 4C PLOT, DEV., UV & PEEL

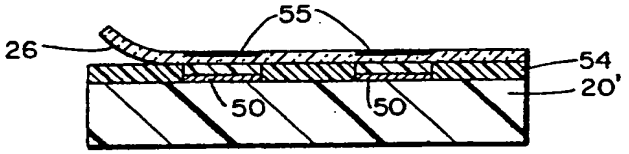


FIG. 4D REMOVE UNEXPOSED PDF

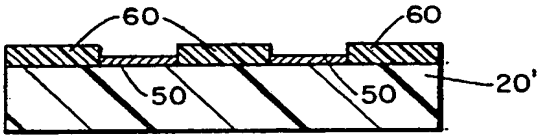


FIG. 4E SOLDER BATH

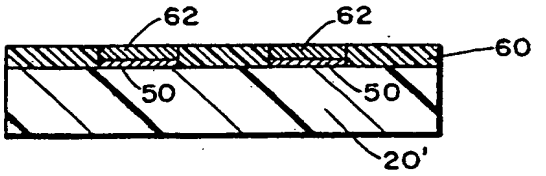


FIG. 4F PLATE UP (ALTERNATIVE STEP AFTER 4D)

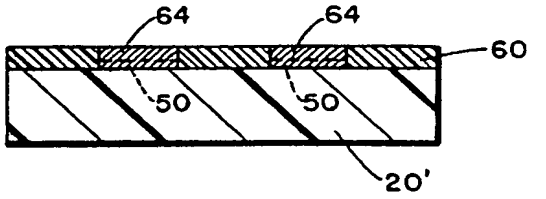


FIG. 5A

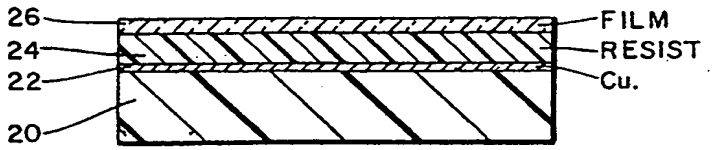


FIG. 5B PLOT, DEV., UV & PEEL

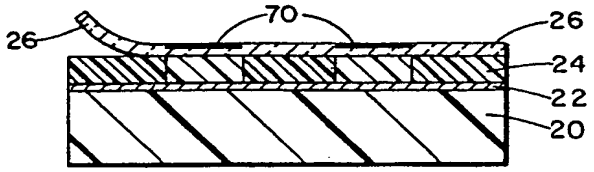


FIG. 5C REMOVE SOFT RESIST

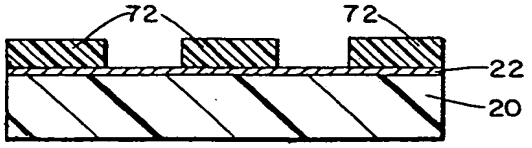


FIG. 5D ELECTROPLATE Cu., TIN-SOLDER

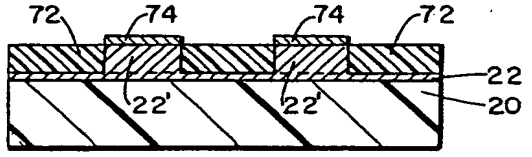


FIG. 5E REMOVE HARD RESIST

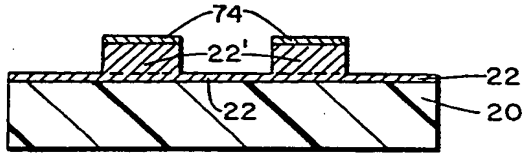


FIG. 5F ETCH BACKGROUND Cu.

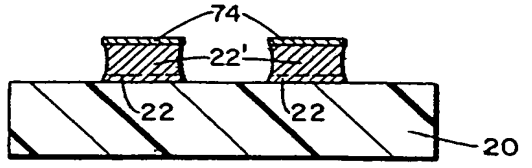


FIG. 6A

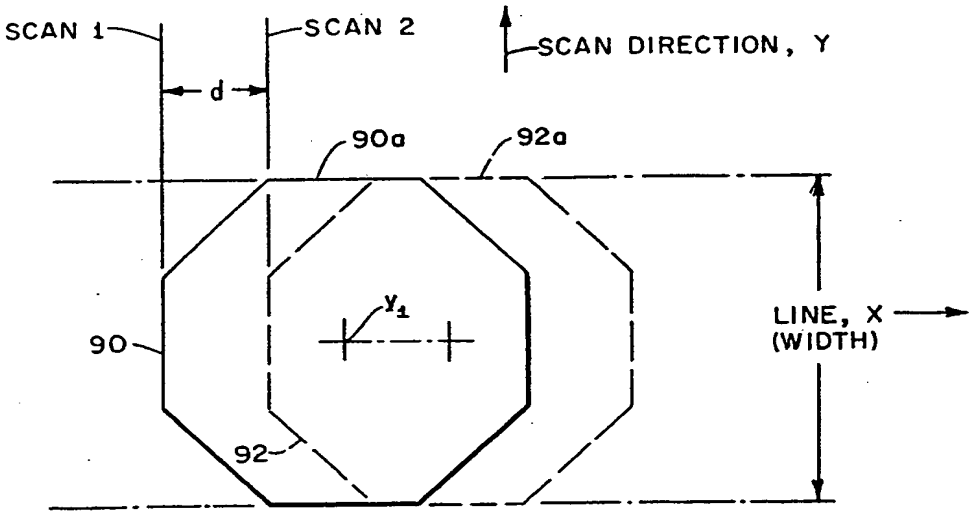

SCAN 1
SCAN 2
SCAN DIRECTION, Y
d
90a
92a
y_1
90
LINE, X
(WIDTH)
92

FIG. 6B

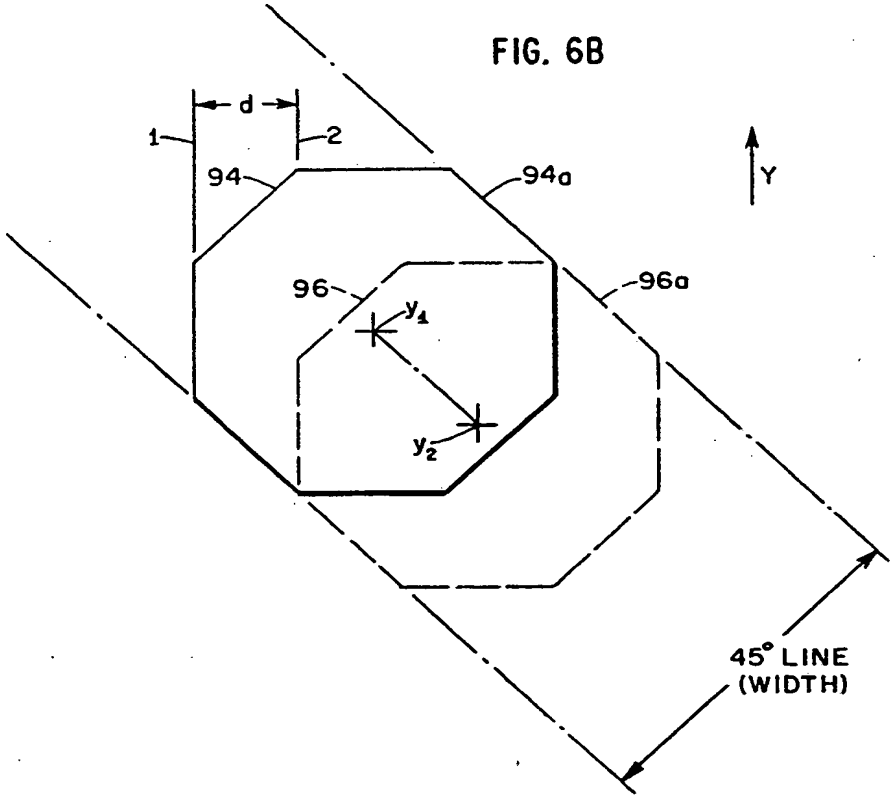

d
1
2
94
94a
Y
96
96a
y_1
y_2
45° LINE
(WIDTH)

FIG. 7A

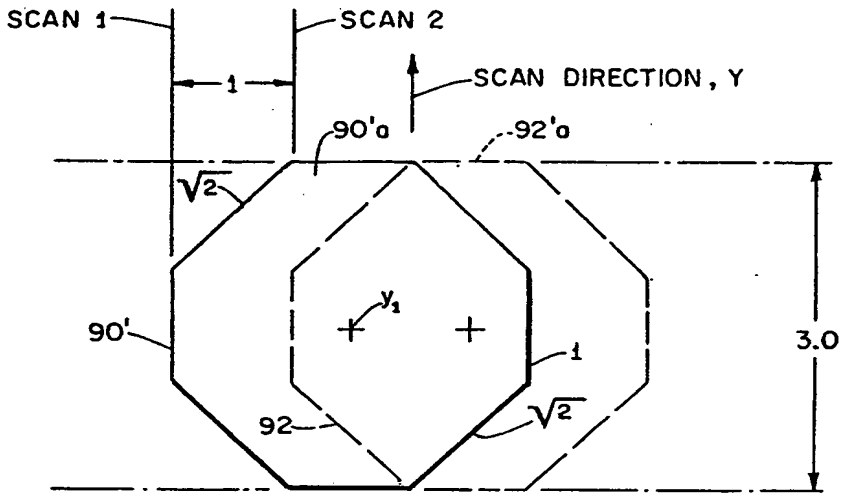
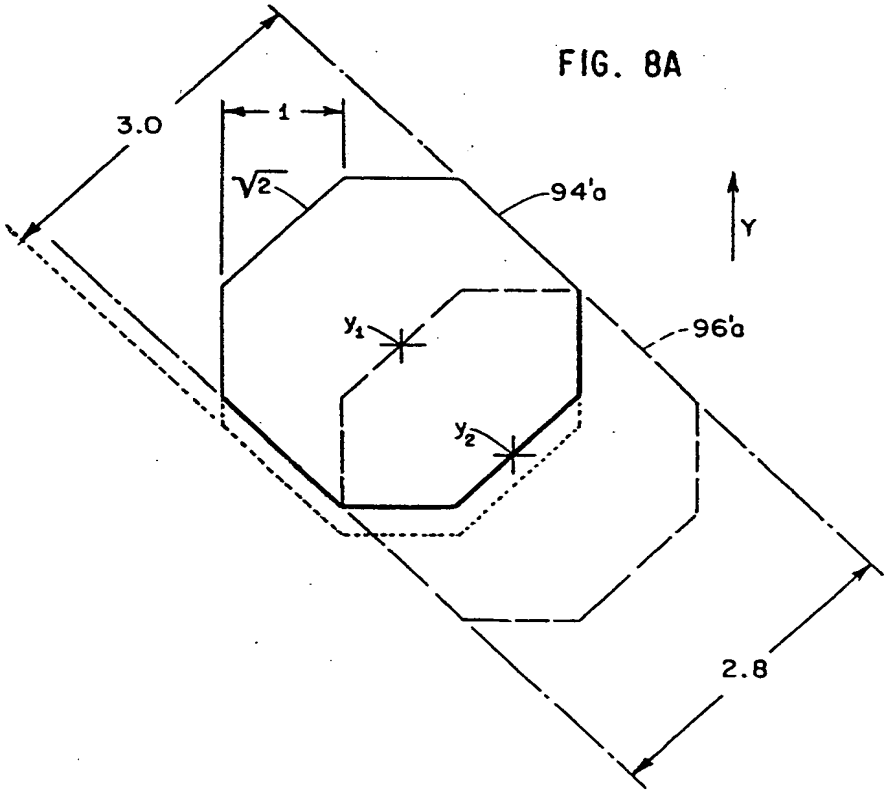

SCAN 1
SCAN 2
1
SCAN DIRECTION, Y
90'a
92'a
√2
y1
90'
1
3.0
92
√2

FIG. 8A


3.0
1
√2
94'a
Y
y1
96'a
y2
2.8